T36014

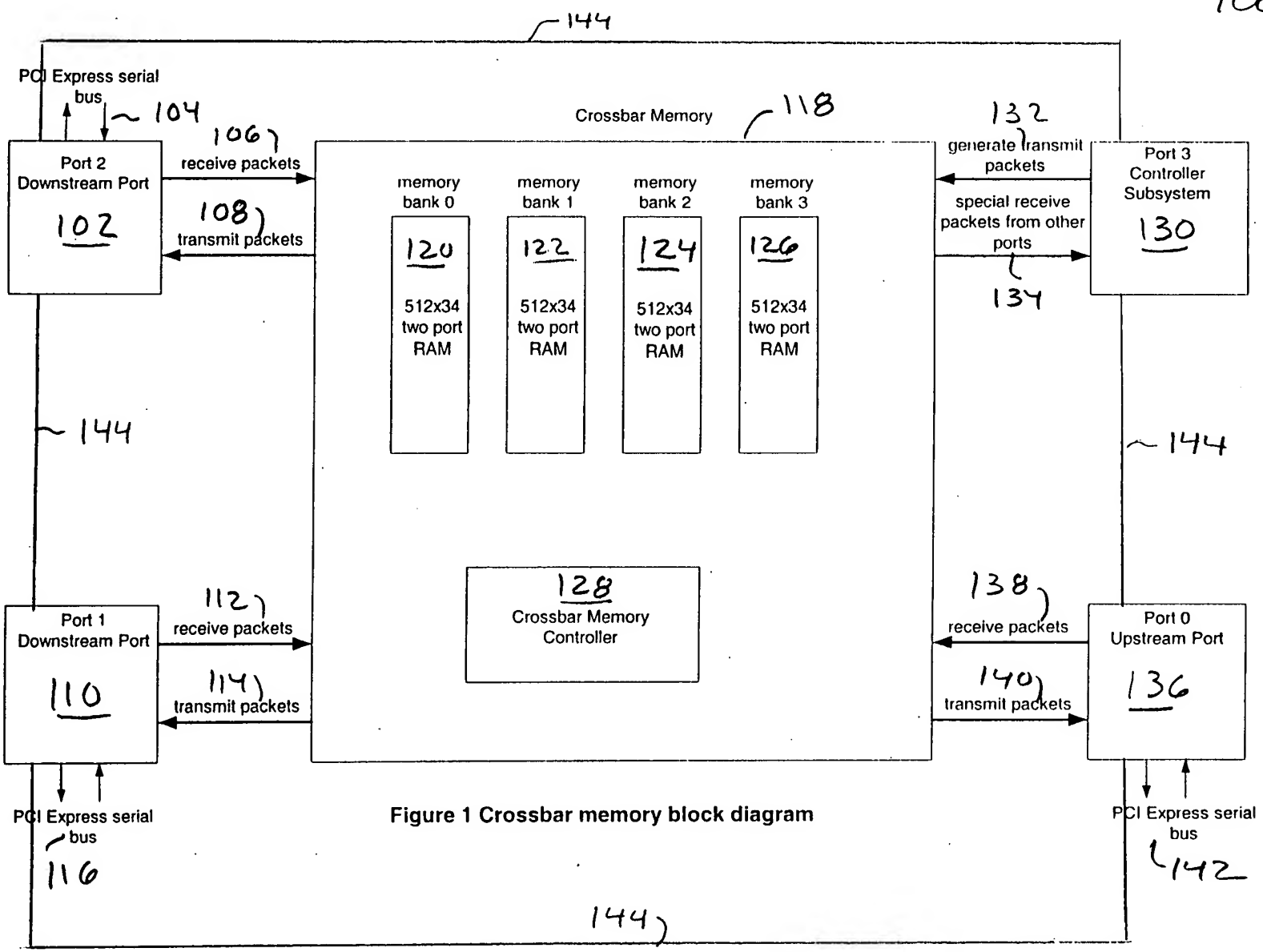


Figure 1 Crossbar memory block diagram

T36014

200

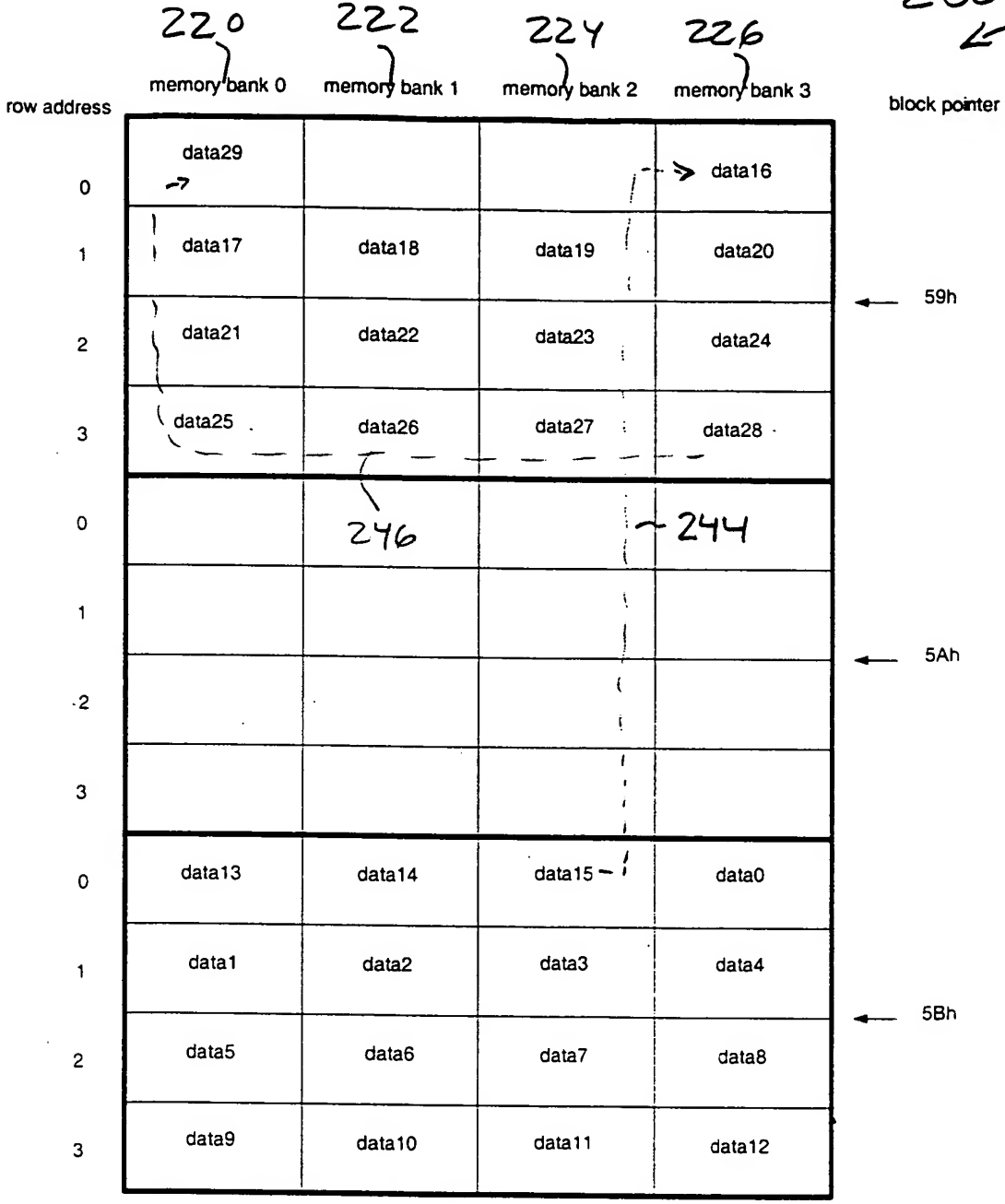


Figure 2 Crossbar memory packet storage

T36014

300)

Cr ssbar mem ry stored data structure

	bit33	bit32	bit31 … bit0	block pointer
POINTER	ptr7(6) = 1	0	data16	
	ptr7(5) = 0	0	data17	
	ptr7(4) = 1	0	data18	
	ptr7(3) = 1	0	data19	
	ptr7(2) = 0	0	data20	
	ptr7(1) = 1	0	data21	
	ptr7(0) = 0	0	data22	
DON'T CARE	0	0	data23	← 59h
	0	0	data24	
	0	0	data25	
	0	0	data26	
	0	0	data27	
	0	0	data28	
	0	1	data29 (end-of-packet status token)	
				← 5Ah
POINTER	ptr7(6) = 1	0	data0	
	ptr7(5) = 0	0	data1	
	ptr7(4) = 1	0	data2	
	ptr7(3) = 1	0	data3	
	ptr7(2) = 0	0	data4	
	ptr7(1) = 0	0	data5	
	ptr7(0) = 1	0	data6	
DON'T CARE	0	0	data7	← 5Bh
	0	0	data8	
	0	0	data9	
	0	0	data10	
	0	0	data11	
	0	0	data12	
	0	0	data13	
	0	0	data14	
	0	0	data15	

Figure 3 PCI Express packet storage data structure

T360014

400

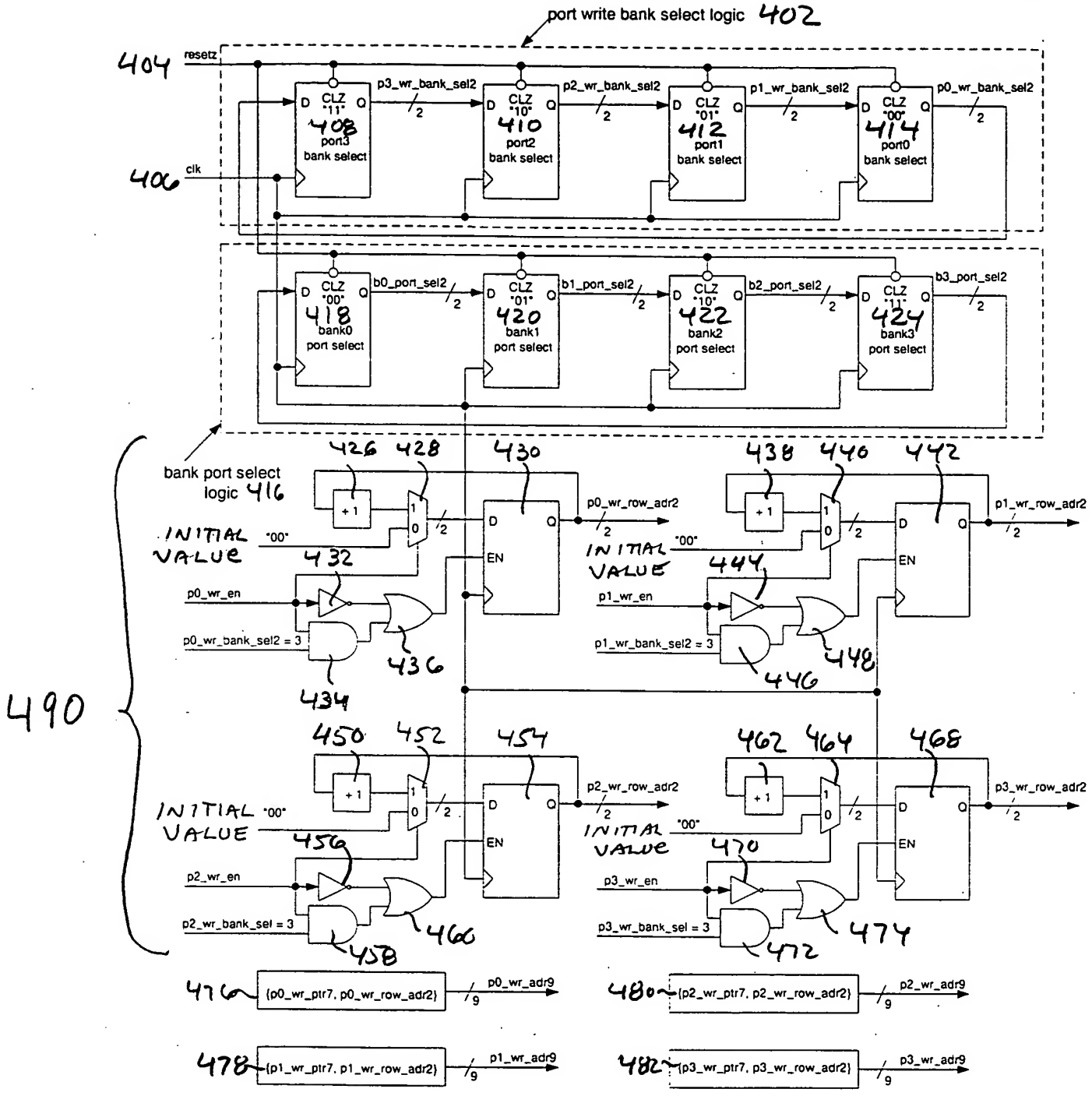


Figure 4 Crossbar memory controller - bank select, port select and write address logic

T36014

500

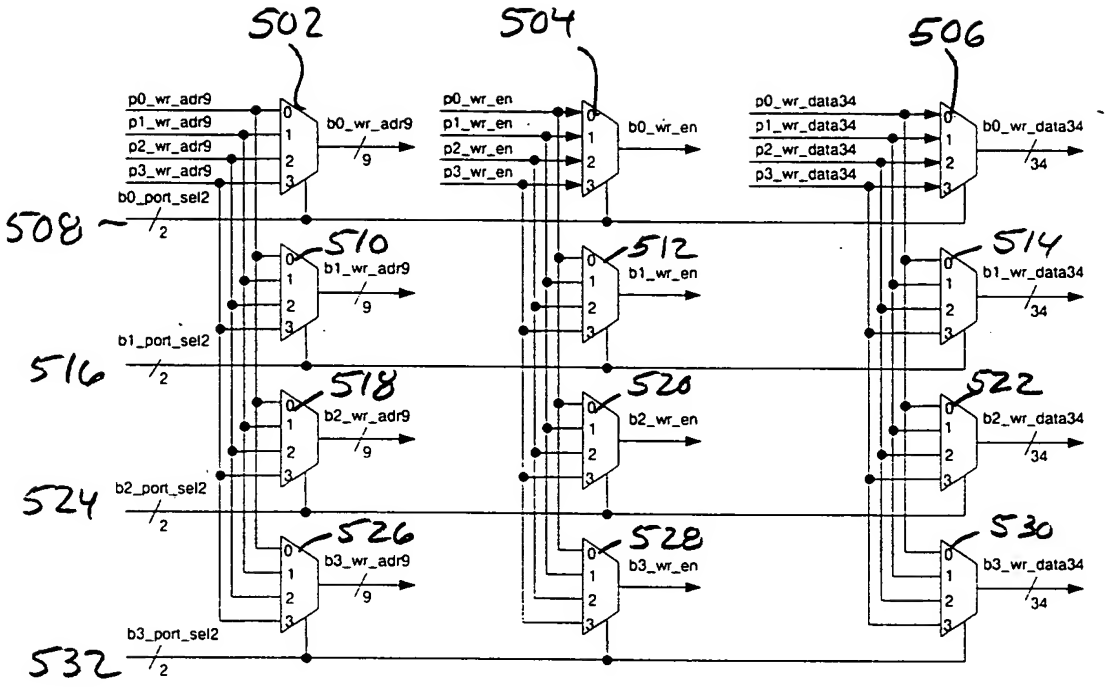


Figure 5 Crossbar memory controller - memory bank write mutiplex logic

T36014

600

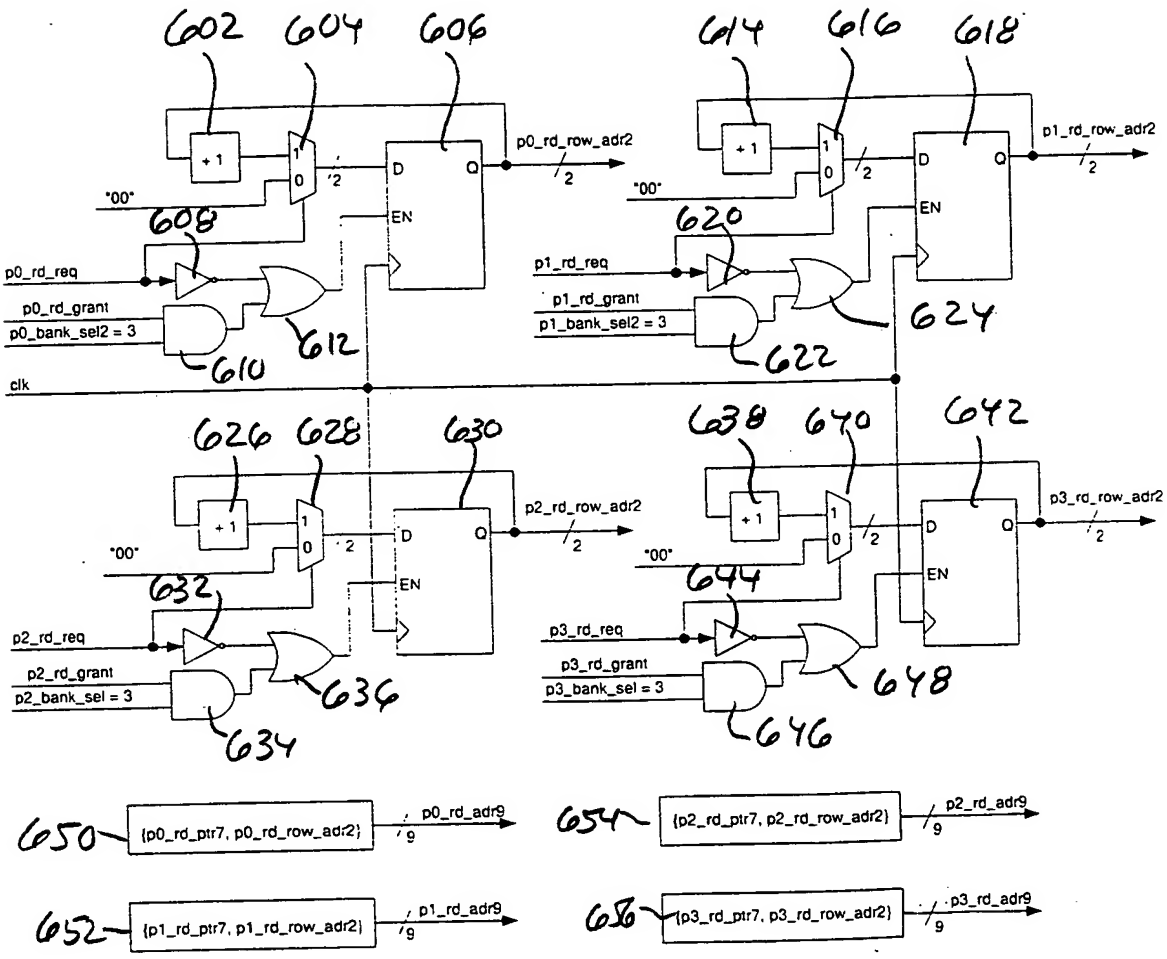


Figure 6 Crossbar memory controller - port read address logic

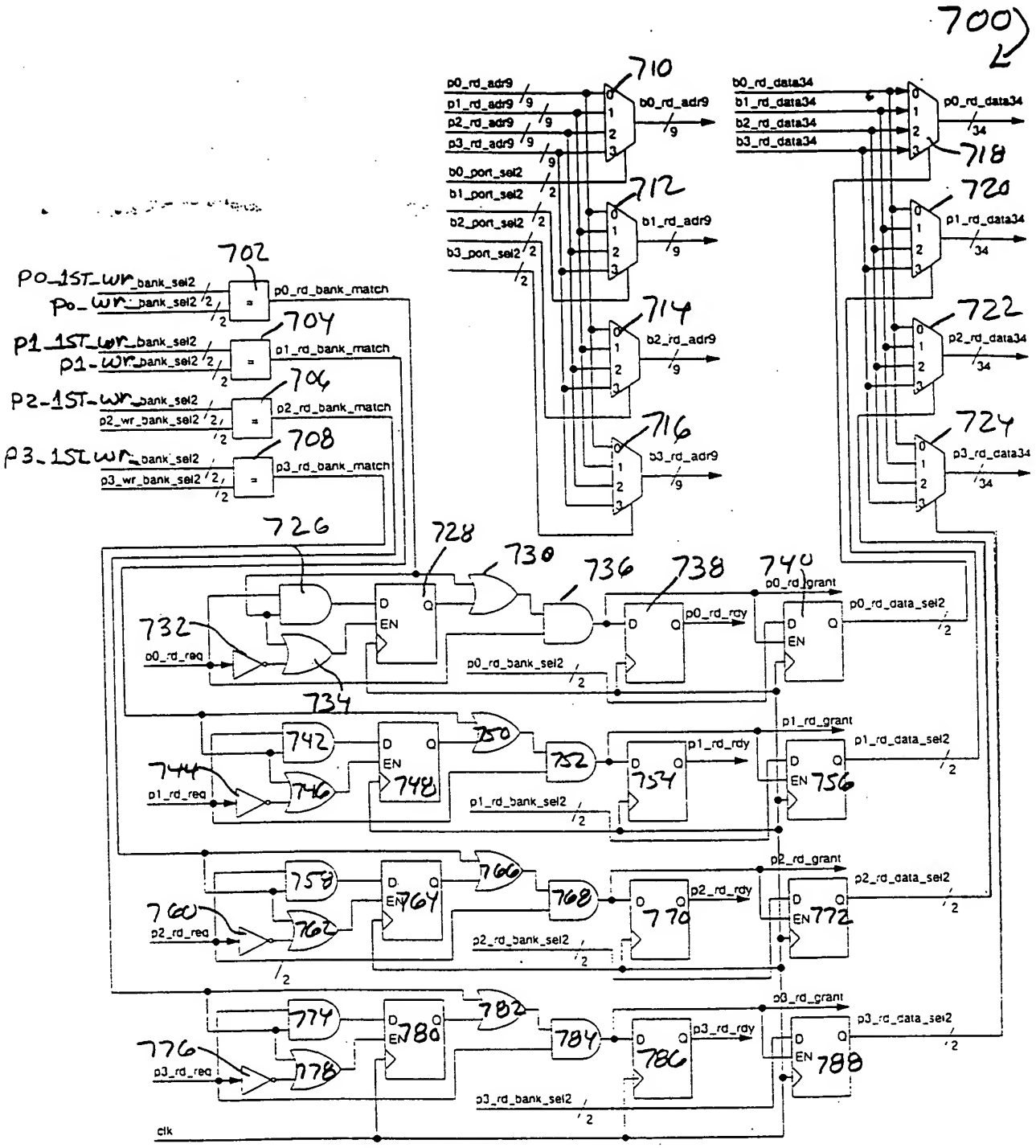


Figure 7 Crossbar memory controller - memory bank read control logic

T36014

800

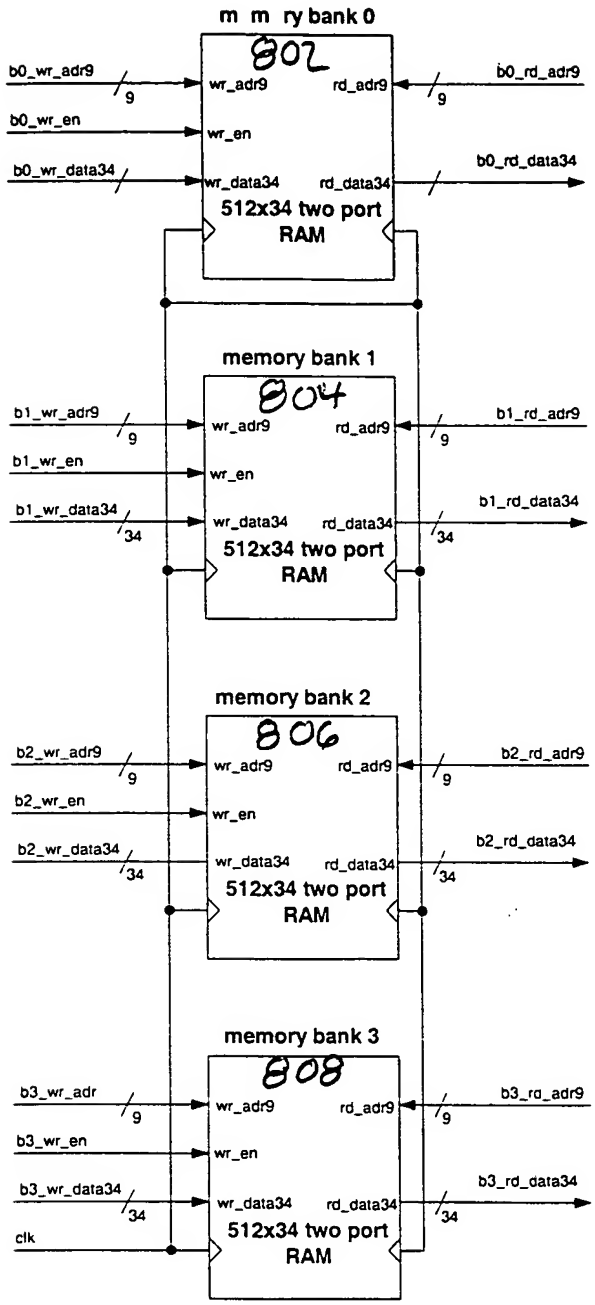
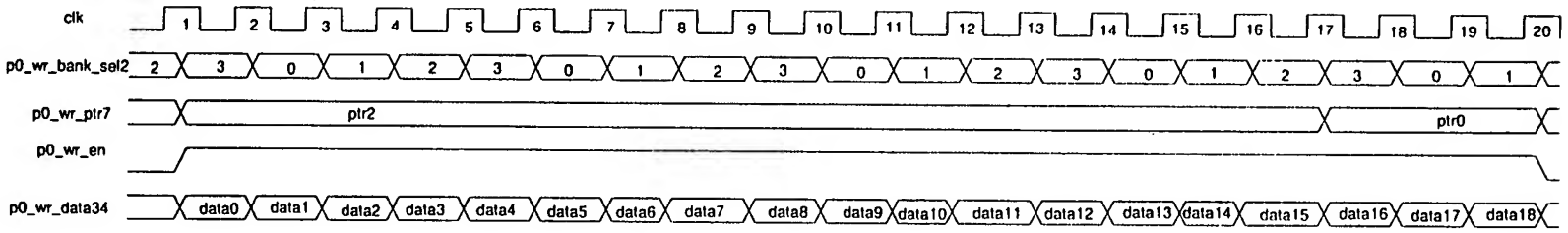


Figure 8 Crossbar memory bank access interface signals

T36014
900



Note:In this example port 0 start writing crossbar memory from memory bank 3

Figure 9 port receive packet write timing diagram

736014
1000

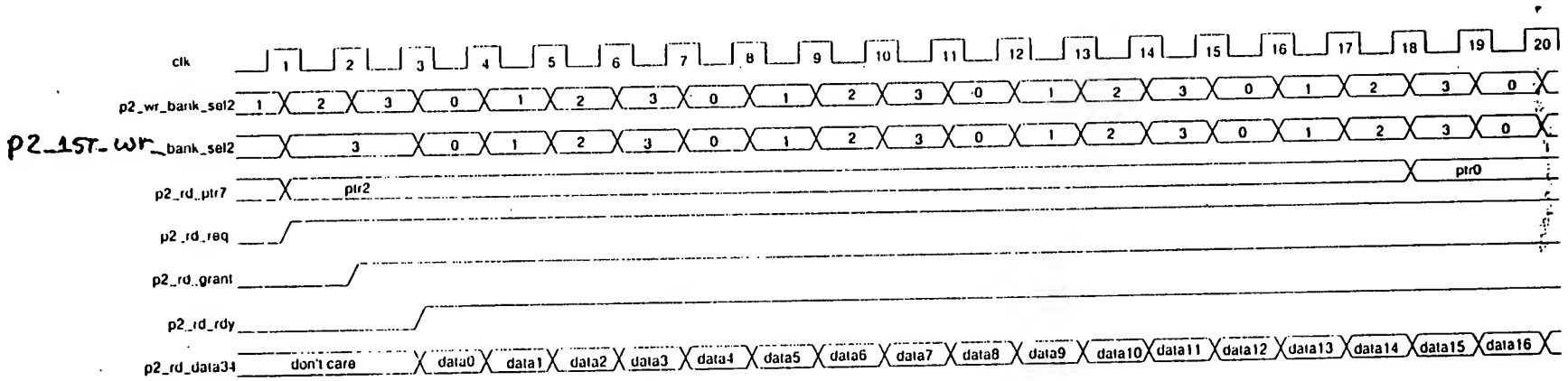


Figure 10 port transmit packet read timing diagram -1

T36014
1109
.2

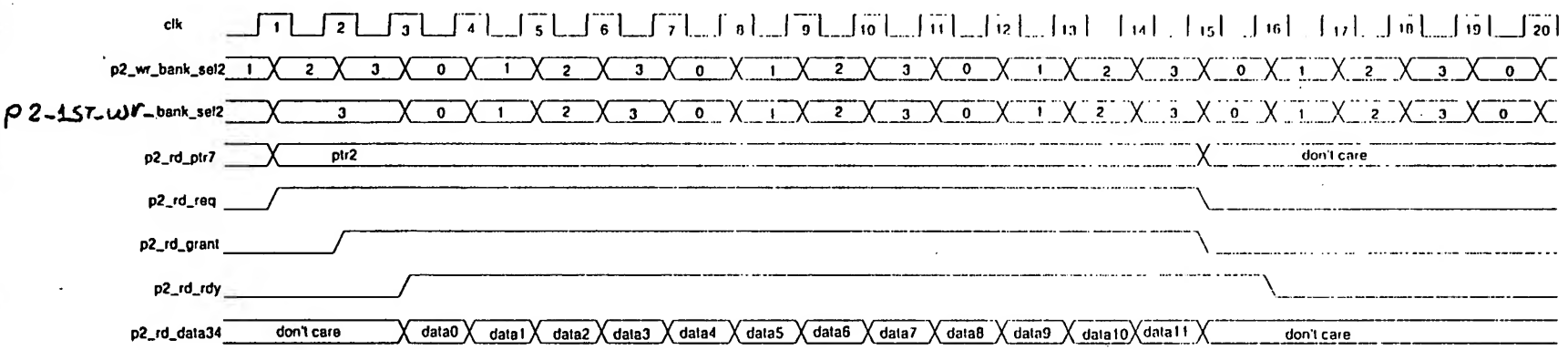


Figure || port transmit packet read timing diagram -2 (shown read termination)

T36014

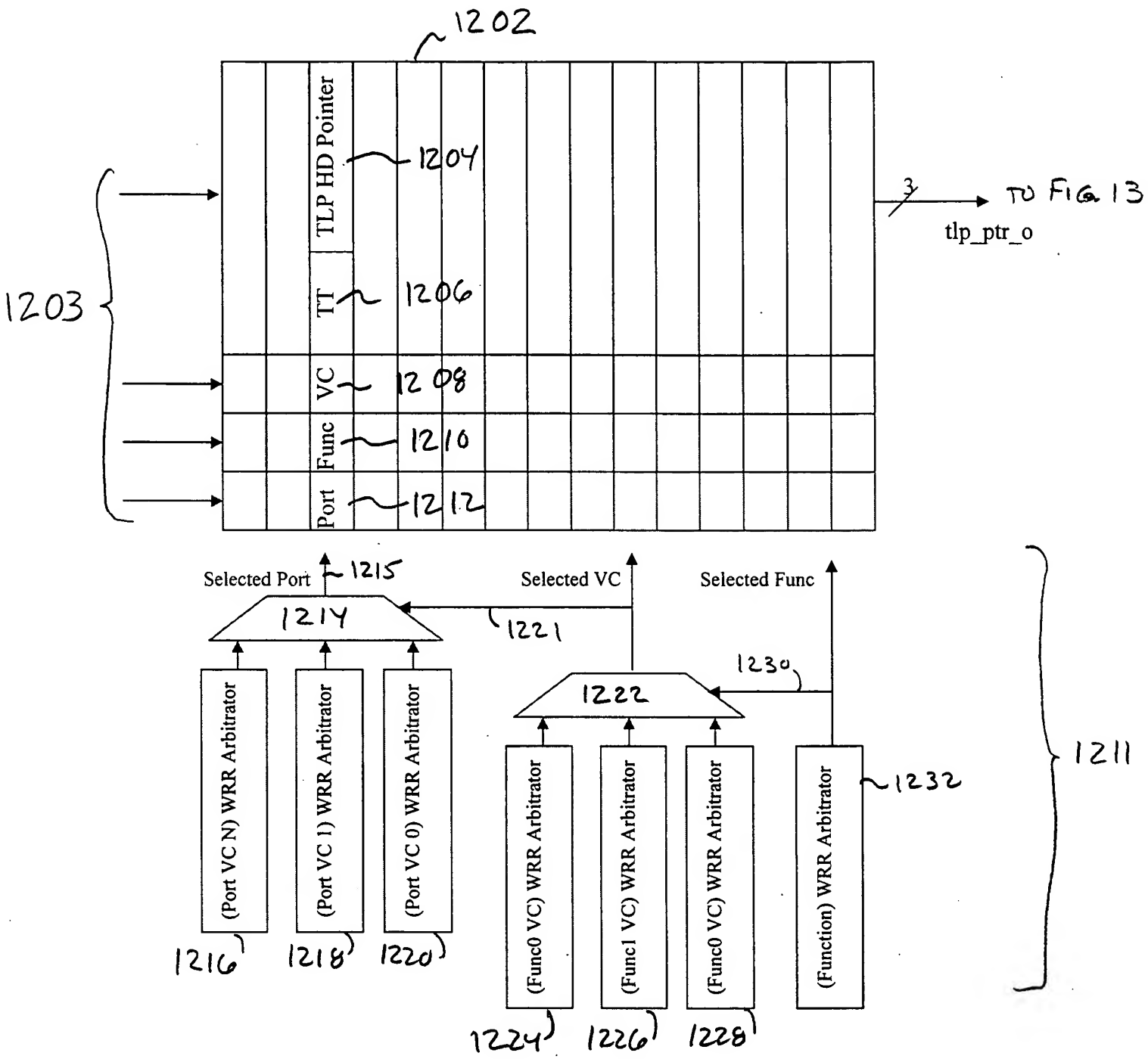


FIG. 12

T36014

1300

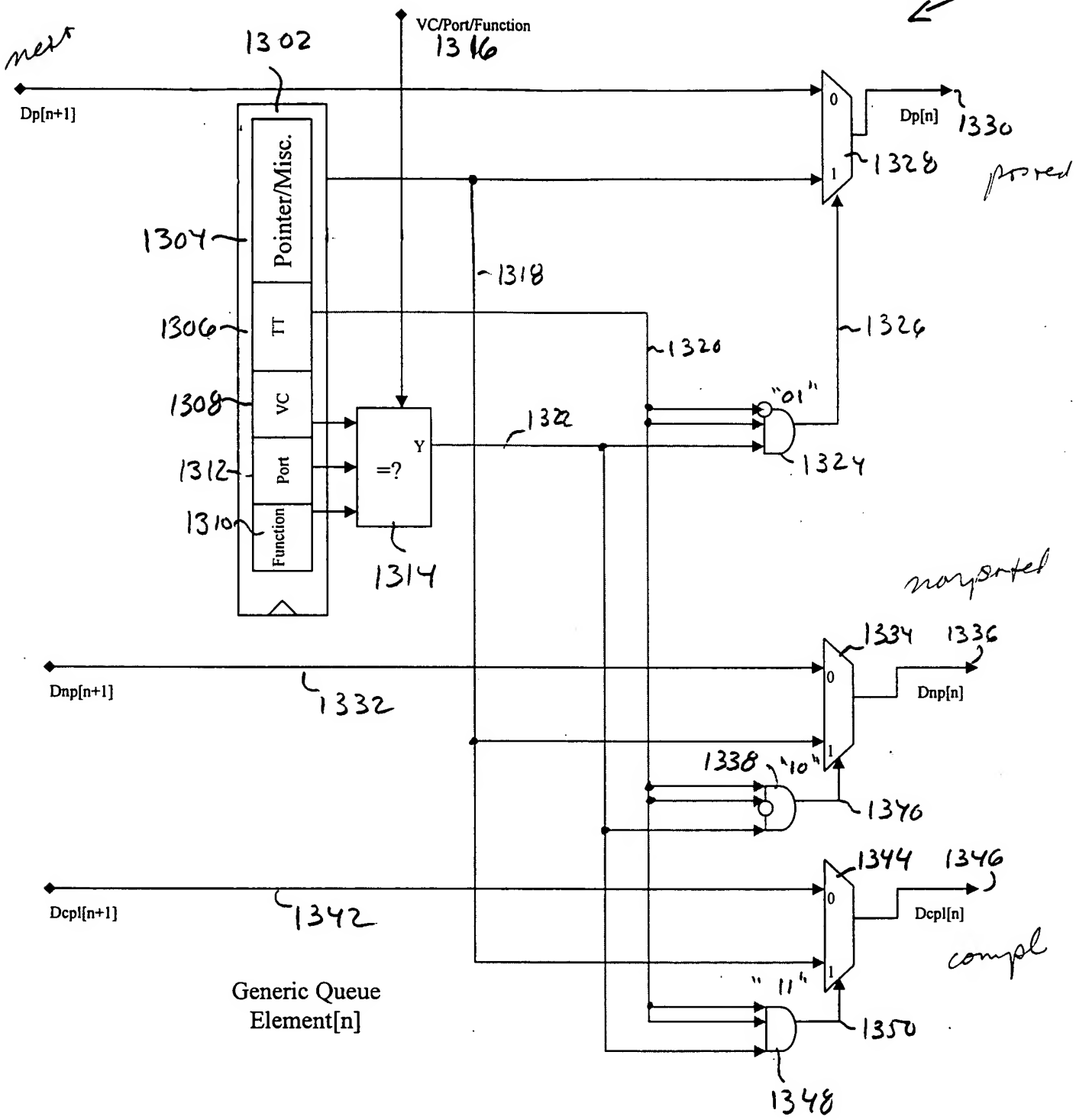


FIG. 13